## AMENDMENTS TO THE CLAIMS

This listing of the claims will replace all prior versions and listing of the claims in this application.

Listing of the Claims:

1 - 12. (Canceled)

13. (previously presented) First and second bipolar transistors formed on a p-substrate, said first transistor comprising:

a Sb subcollector;

a n-epi collector;

a SiGe polysilicon p-doped extrinsic base;

a SiGe silicon single crystal intrinsic base; and

said second transistor comprising:

an As subcollector having a sheet resistance at 50-200 Ω/square;

a n-epi collector;

a SiGe polysilicon extrinsic base; and

a SiGe single crystal extrinsic base, said second transistor providing ESD protection as a result of the selection of As as a subcollector which provides for lateral ballasting.

14. (Original) The semiconductor structure of claim 13, further comprising a polysilicon emitter.

15. (Canceled)

16. (Withdrawn) A method for manufacturing a semiconductor device on a wafer comprising the following steps:

forming a first subcollector region in the wafer;

forming a second subcollector region in the wafer; wherein the second subcollector differs from the first subcollector;

forming an isolation structure abutting an end portion of at least one subcollector region;

forming a SiGe film or SiGeC film on the wafer surface above said first and second subcollector regions for formation of a transistor base region;

forming an emitter structure on the SiGe or SiGeC film.

17. (Withdrawn) The method of manufacturing a semiconductor device of Claim 16, wherein the first subcollector implant differs from the second subcollector region in impurity type or doping concentration.

18. (Withdrawn) The method of manufacturing a semiconductor device of Claim 16, wherein a first bipolar transistor is formed on said first subcollector region and a second bipolar transistor is formed on said second subcollector region.

19. (Withdrawn) A method of manufacturing a semiconductor device on a wafer comprising the following steps:

forming a subcollector region by implantation of the wafer with a first dopant and with a second dopant;

forming an isolation structure on the subcollector region;

forming a SiGe film or SiGeC film on the wafer surface for formation of a transistor base region;

forming an emitter structure on the SiGe or SiGeC film.

20-22. (Canceled.)